ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

M.TECH. VLSI AND EMBEDDED SYSTEMS

Course of Study & Scheme of Examination
2016-17

Maulana Azad National Institute of Technology
Bhopal

SCHEME

M.TECH. IN VLSI & EMBEDDED SYSTEM DESIGN

SEMESTER: I

Course No.	Subject Name	Scheme Of Studies Per Week			Distribution Of Credit
		L	T	P	Total
VED-511	VLSI Technology	3	0	0	3
VED-512	VLSI Design	3	0	0	3
VED-513	Embedded Systems	3	0	0	3
	Department Elective - 1	3	0	0	3
	Department Elective - 2	3	0	0	3
	Open Elective - 1	3	0	0	3
VED-514	VLSI Lab	0	0	3	2
VED-515	Seminar I	0	0	3	2
	Total				**22**

SEMESTER: II

Course No.	Subject	Scheme of studies periods per week			Distribution Of Credits
		L	T	P	Total
VED-521	Low power VLSI Design	3	0	0	3
VED-522	Physical Design Automation	3	0	0	3
VED-523	Testing of VLSI circuits	3	0	0	3
	Department Elective - 3	3	0	0	3
	Department Elective - 4	3	0	0	3
	Open Elective - 2	3	0	0	3
VED-524	System Design Lab	0	0	3	2
VED-525	Seminar II	0	0	3	2
				Total	**22**

ELECTIVE SUBJECTS FOR SEMESTER: I and II

(Department Elective) DE (Two DE per Semester)	VED-531 Digital System Design VED-532 Mixed Signal Design VED 533 Design of Testability VED 534 Design of Semiconductor Memories VED 535 CMOS Active Filter Design VED-536 Design of Analog IC VED-537 CMOS RF Circuit Design VED 538 Device Modelling and Simulation
(Open Elective) OE (One OE per Semester)	VED-551 Computational Techniques in Digital Syste Design VED 552 Optimization Techniques VED 553 High Speed System Design VED-554 CAD of Digital System VED 555 Selected Topics in VLSI VED-556 Advance Computer Architecture VED-557 Fuzzy Logic VED-558 Neural Networks

SYLLABUS

VED-511 VLSI TECHNOLOGY

Design and Technology overview, Fabrication process – crystal growth, epitaxy, oxidation, lithography, etching, film deposition, diffusion, ion implantation, metallization.

VLSI process integration – NMOS, CMOS, BJT. Assembly techniques, packing of VLSI devices.

References:

1. C.Y. Chang and S.M.Sze ,"ULSI Technology", McGraw Hill.
2. S.K. Ghandhi, "VLSI Fabrication Principles", John Wiley Inc.
3. S.M. Sze ,'VLSI Technology", McGraw Hill.

VED-512 VLSI DESIGN

Introduction of VLSI Design Methodologies – Design Description domains, Introduction to HDL – HDL Design Examples, CMOS Circuits & Logic design – basic physical design of simple logic gates, CMOS logic Structures – BiCMOS logic, pseudo nMOS, dynamic CMOS, clocked CMOS, Pass transistor logic, CMOS domino, NP-domino logic, clocking strategies, I/O Structures, System design and methods – CMOS design methods, CMOS design options, layout and stick diagrams.

References:

1. Nei l H.E. Weste & Kamraneharghian , “Principles of CMOS VLSI design” . Add Nesly Pub.
2. Jacob baker, Harry Wili & David Boyce , “CMOS Circuit design”.

VED-513 EMBEDDED SYSTEMS

Introduction to Embedded Hardware Elements, Sensors and Actuators, Embedded Processors, Memory Architectures.

Microprocessor interrupts architecture – Shared data problem and its solutions, interrupt latency. Introduction to Embedded Software Architectures, Real Time Operating Systems - Task and Task States, Semaphores and shared Data, RTOS services and design using RTOS, RTOS function calls.

Introduction to Embedded System Development tool chain and integrated development environment (IDE). Software development with PIC Micro-controller and Interfacing.

References:

1. E. A. Lee and S. A. Seshia, “Introduction to Embedded Systems - A Cyber-Physical Systems Approach”, Second Edition, LeeSeshia.org, 2015.
2. David E Simon, “An embedded software primer” , Pearson education Asia, 2001.
3. John B Peat man, “Design with PIC micro-controllers”, Pearson education Asia, 1998.

VED-521 LOW POWER VLSI DESIGN

Introduction to Low power CMOS VLSI design. Sources of power dissipation. Leakage reduction techniques: process level and circuit level. Design time techniques.Run time stand by techniques. Architecture level static voltage scaling (pipelining and parallelism used for low power design). Voltage scaling with optimal transistor sizing, high level circuit transformation, Switched capacitance minimization techniques. low power static RAM architecture, software design for low power, Case studies.

References:

1. Gary Yeap , “Practical Low Power Digital VLSI Design”, 1997.
2. Kaushik Roy, Sharat Prasad , “Low Power CMOS VLSI Circuit Design”, 2000

VED-522 PHYSICAL DESIGN AUTOMATION

VLSI physical design automation – VLSI design cycle, design style, system packaging style, impact of fabrication process on physical design. Floorplanning and Pin Assignment, Placement – problem formulation, partitioning based placement problems, Global routing – problem formulaton Detailed Routing – multilayer routing algorithms, Over the cell routing and via minimization, Clock and power routing, PDA of FPGAs and MCMs.

References:

1. N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”, 1999.
2. Sadiq M Sait, “VLSI Physical Design Automation: Theory and Practice” .

VED-523 TESTING OF VLSI CIRCUITS

Introduction to VLSI testing process and test equipment, Test Economics and Product Quality, Defect Level Estimation, Fault Modeling – Introduction Fault Models, Single Stuck-at Fault, Fault Collapsing, Logic and Fault simulation – Algorithms for True-Value Simulation and for Fault Simulation. Testability Measures – SCOAP measures, Combinational circuit test generation, sequential circuit test generation, Basics of ATPG Algorithms – Roth's D-Calculus and D-Algorithm, Introduction to DFT fundamentals.

References:

1. Viswani D. Agrawal Michael L. Bushnell, "Essentials of Electronic Testing for digital memory and mixed signal VLSI circuit", Kluwer Academic Publications, 1999.
2. Alfred L. Crouch, "Design for test for digital ICs and embedded core systems", PHI 1999.

VED-531 DIGITAL SYSTEM DESIGN

Sequential Logic Design- Introduction, Basic Bistable Memory Devices, reduced characteristics and excitation table for bistable devices. Synchronous Sequential Logic Circuit Design- Introduction, Moore, Mealy and Mixed type, Synchronous State Machines. Synchronous sequential design of Moore, Mealy Machines, Synchronous Counter Design, Hazards, Duality of sequential circuits, Different methods of inimization.Asynchronous Sequential logic design- Introduction, Primitive flow table and reduction, type of delays, Cycles and races, Excitation Map, Hazards, Essential hazards, Analysis of asynchronous sequential circuits. Symmetric and Iterative circuits- Symmetric functions, iterative functions, realization in tree form. Algorithmic State Machine- An Algorithm with inputs, digital solution, Implementation of traffic light controller, ASM charts, Design Procedure for ASMs. Introduction to programmable logic devices-PALs,PLDs,CPLDs,FPGAs.

References:

1. M.Morris Mano, “Digital Design”, 3rd edition, Pearson Education.
2. Charles H.Roth, Jr. “Fundamentals of Logic Design”, 4th Edition, Jaico Publishing House
3. Donald D.Givone, “Digital Principles and Design”, Tata McGraw-Hill.
4. Stephen H. Unger, “The Essence of Logic Circuits”, 2nd Edition Wiley-IEEE Press

VED-532 MIXED SIGNAL DESIGN

Fundamental circuit techniques and design issues for mixed-signal integrated circuits. approximation ADCs, Dual slope ADCs, High-speed ADCs (e.g. flash ADC, pipeline ADC and related architectures), High-resolution ADCs (e.g. delta-sigma converters), Data converters – SNR, Noise shaping, Bandpass data converters, high speed data converters, , analog switches, comparators.

References:

1. R. Jacob Baker,John “CMOS: Mixed-Signal Circuit Design”, Wiley & Sons Inc. , IEEE Press, 2nd Edition, 2009
2. Rudy V. dePlassche. “CMOS Integrated ADCs and DACs” , Springer, Indian edition
3. Thomas H. Lee, “The Design of CMOS Radio-Frequency Integrated Circuits”, , Cambridge University Press, Second Edition, 2004.

VED-533 DESIGN OF TESTABILITY

Review of Testing Process, Test Economics and Test Methods, Digital DFT and Scan Design – Scan Design Rules, Overheads of Scan Design, Built-In Self-Test – BIST Process, Pattern Generation, Device Level BIST, Boundary Scan Standards, BSDL, Analog Test Bus Standard, System Test and Core-based Design.

References:

1. Viswani D. Agrawal Michael L. Bushnell, “Essentials of Electronic Testing for digital memory and mixed signal VLSI circuit”, , Kluwer Academic Publications, 1999.
2. Alfred L. Crouch, “Design for test for digital ICs and embedded core systems”– PHI 1999.

VED-534 DESIGN OF SEMICONDUCTOR MEMORIES

Random Access Memory Technologies, silicon on insulator (SOI) technology advanced SRAM architectures and technologies, application specific SRAMs, Dynamic Random Access Memories (DRAMs), Advanced DRAM designs and architecture – application specific DRAMs.

Nonvolatile Memories, Memory fault modeling, testing and memory design for Testability and fault tolerance, Semiconductor memory reliability and radiation effects, advanced memory technologies and high-density memory packaging technologies, CD, Blueray disk.

References:

1. Ashok K.Sharma, “Semiconductor Memories Technology, testing and reliability”,, Prentice hall of India Private Limited, New Delhi 1997.
2. Gerald Luecke, “Semicoductor memory design and application”,McGraw-Hill.
3. **Ashok K. Sharma,** “**Advanced Semiconductor Memories: Architectures, Designs, and Applications”,**Wiley

534 Design of Semiconductor Memories

VED-535 CMOS ACTIVE FILTER DESIGN

Introduction of Filters at mixed signal system, Analog filter, Filter approximation- Magnitude, Phase, group delay. Continuous-time, Discrete-time types of filters. Designing of filter Active-RC, MOSFET-C, Gm-C, Gm-Opamp-C, Switched-capacitor, switched-current filter. Noise in active RC filters, Adaptive Filters, Higher order filters and cascade, switched capacitor filters. Scattering parameter models, analysis and applications

References:

1. C. Toumazou, F. J. Lidgey, “Analogue IC Design: The Current-Mode Approach” (IEE Circuits and Systems Series)
2. The Circuits and Filters Handbook, Second Edition, Wai-Kai Chen CRC Press
3. Electronic Filter Design Handbook by Arthur B. Williams, McGraw-Hill

VED-536 DESIGN OF ANALOG IC

Introduction to analog VLSI, Common Source Amplifier, Small Signal Modeling, Source Follower; Common Gate; Cascode, Current Mirror; Channel Length Modulation, Common Source Amplifier, Active Load, Frequency Response; Bandwidth of Common Source Amplifiers, Differential Pair, Active Load, Stability of Closed Loop Op-Amp, Op-Amp Compensation; Miller Effect, Noise Fully Differential Op-Amps.Noise,stability and frequency compensation, Switched Capacitor Circuits

References:

1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits” , McGrawHill,
2. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer , “Analysis and Design of Analog Integrated Circuit”, John Wiley & Sons, Inc. 4th edition.
3. Willy Sansen, “Analog Design Essentials”, Springer, 2006.

VED-537 CMOS RF CIRCUIT DESIGN

Introduction and Applications of RF Transceiver, Basic Concepts in RF Design, Random processes and noise , sensitivity - dynamic range, conversion of gains and distortion. Receiver and Transmitter Architectures. Modeling and behavior of MOSFET at RF frequencies, Integrated parasitic elements at high frequencies and their monolithic Implementation.Basic blocks in RF systems and their VLSI implementation: Low Noise Amplifier design with CMOS, design of mixers at GHz frequency range, Oscillators – ring oscillator, LC oscillator, VCO designs, radio frequency synthesizers , PLL.

References:

1. B. Razavi , “RF Microelectronics”, Prentice Hall of India
2. R. Jacob Baker, H.W. Li and D.E. Boyce, “CMOS Circuit Design, Layout and Simulation”, Prentice Hall of India.
3. Thomas H. Lee “Design of CMOS RF Integrated Circuits”, Cambridge University press.
4. Y.P. Tsividis, “Mixed Analog and Digital VLSI Devices and Technology”, McGraw Hill.

VED-538 DEVICE MODELLING AND SIMULATION

Integrated circuits diodes and transistors; Current-voltage characteristics; Ebers-Moll model and Gummel-Poon model of bipolar transistors; current gain; Early effect and high level injection; 2-D effects; transient parameters; MOSFETs; analysis of MOSFET parameters; short channel and narrow width effects; hot electron effects; MOSFET models; JFET and MESFETs; Modulation doped FETs, HEMTs; Heterojunctions and HBTs; microwave and optonic devices; outline of numerical approach to 2D and 3D device models; Introduction to device simulation programs.

References:

1. Nandita DasGupta and Amitava DasGupta, “Semiconductor Devices”, PHI.
2. S. M. Sze, “Physics of Semiconductor Devices”, John Wiley & Sons.
3. Karl Hess, “Advanced Theory of Semiconductor Devices”, IEEE Press

VED-551 COMPUTATIONAL TECHNIQUES IN DIGITAL SYSTEM DESIGN

Linear algebra, Lagrange multipliers. Differential equations of equilibrium; Laplace's equation and potential flow; boundary-value problems; minimum principles and calculus of variations. Digital systems modeling and simulation,Integrated logicBoolean algebra and logic,Logic function optimization,Number systems,Combinational logic,VHDL design concepts,Sequential and synchronous sequential logic

References:

1. Strang, Gilbert., "*Computational Science and Engineering.*",Wellesley, MA. Wellesley-Cambridge Press,
2. Mohammed Ferdjallah, "Introduction to Digital Systems: Modeling, Synthesis, and Simulation Using VHDL"

VED- 552 OPTIMIZATION TECHNIQUES

Motivation. mathematical review , matrix factorizations, sets and sequences, convex sets and functions, linear programming and simplex method, Weierstrass' theorem, Karush Kuhn Tucker optimality conditions, algorithms, convergence, unconstrained optimization, Line search methods, method of multidimensional search, steepest descent methods, Simplex algorithm, Gradient Search Methos, Newton's method, modifications to Newton's method , trust region methods, conjugate gradient methods, quasi-Newton's methods. constrained optimization, penalty and barrier function methods, augmented Lagrangian methods, polynomial time algorithm for linear programming, successive linear programming, successive quadratic programming.

References:

1. R. Fletcher, “Practical Optimization”, (2nd Edition) John Wiley & Sons, New York, 1987.
2. M.S.Bazaraa , H.D.Sherali and C.Shetty, “Nonlinear Programming, Theory and Algorithms” , John Wiley and Sons, New York, 1999

VED- 553 HIGH SPEED SYSTEM DESIGN

Transmission line theory (basics), crosstalk effects; signal integrity: impact of packages, vias, traces, connectors; non-ideal return current paths, high frequency power delivery, simultaneous switching noise; system-level timing analysis and budgeting; methodologies for design of high speed buses; radiated emissions and minimizing system noise; Practical aspects of measurement at high frequencies;

Printed Circuit Board - CAD tools for PCB design, Standard fabrication, Surface Mount Technology, Through Hole Technology, Process Control and Design challenges. Thermal Management, Heat transfer fundamentals, Thermal conductivity and resistance, Conduction, convection and radiation, Cooling requirements.

Reliability - Basic concepts, Environmental interactions. Thermal mismatch and

fatigue failures thermo mechanically induced electrically induced chemically induced. Electrical Testing: System level electrical testing, Design for Testability basics.

IC packaging - Requirements and properties; materials and substrates; wire-bonding;

chip and wafer-level packaging; impact on reliability and testability

References:

1. Stephen H. Hall, Garrett W. Hall, James A. McCall ,“High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices”, , August 2000, Wiley-IEEE Press
2. Tummala, Rao R., “Fundamentals of Microsystems Packaging”, McGraw Hill, 2001
3. R.G. Kaduskar and V.B.Baru” ,Electronic Product design”, Wiley India, 2011

VED-554 CAD OF DIGITAL SYSTEM

Introduction to VLSI Methodologies, Design domains and actions. Design methods and technologies. VLSI design automation tools – structural and transistor level design algorithmic and system design , algorithmic graph theory and computational complexities

Tractable and intractable problems, general purpose methods for combinational optimization, Layout compaction, Placement and partitioning, Floor planning concepts, Routing definition and concept.

Simulation – general remarks on VLSI simulation, gate level modelling and simulation switch level modeling and simulation logic synthesis and verification, high level synthesis.

References:

1. S.H. Gerez, “Algorithms for VLSI Design Automation”, 1998.
2. Giovanni De Micheli ,“Synthesis And Optimization Of Digital Circuits”.
3. N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”, 1999.

VED-555 SELECTED TOPICS IN VLSI

Transformation from High level Specifications to VLSI Design, VLSI-SoC design methods, Temperature aware design for multi-core systems, Platform-based design approaches, Compilers for multi-core design, workload distribution in multi-core designs, languages for Embedded Systems and their Applications, frameworks and methodologies for system level approach, system-on-chip test architecture, Safety, reliability and security issues in system design.

References:

1. T. Noergaard, Newnes, “Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers”.
2. D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, “Embedded System Design: Modeling, Synthesis, Verification”, Springer, 2009.

VED-556 ADVANCE COMPUTER ARCHITECTURE

Evolution of computer architecture, taxonomy and models of computers, Instruction set architecture, CISC, RISC processors, pipelined, superscalar , VLIW architecture, case studies, virtual memory technology, Cache memory organization, cache performance, Linear and nonlinear pipelines, Multiprocessors system interconnect, cache coherence and synchronization, message passing mechanisms

References:

1. Kai Hwang. “Advanced Computer Architectur” , (Mc Graw Hill), Edition 1993.
2. M.J. Flynn, “Computer Architecture: Pipelined and Parallel Processor Design”, Publishing Year: Reprint 2011, Narosa Publications.
3. J.Hyaes, “Computer Architecture & Organization”, (Mc Graw Hill), Edition 1989.

VED-557 FUZZY LOGICS

Introduction to fuzzy set theory, Classical sets and fuzzy sets, classical relations and fuzzy relations, membership functions, Fuzzification and Defuzzification, Development of membership functions, Fuzzy logic and Fuzzy systems, Decision making with fuzzy information, Fuzzy clustering, classification and pattern recognition, Fuzzy arithmetic, Engineering Applications of Fuzzy systems.

References:

1. Timothy J. Ross, “Fuzzy Logic with Engineering Applications”, 3rd Edition, Wiley Publications 2010.
2. George J. Klir, Bo Yuan, “Fuzzy Sets and Fuzzy Logic: Theory and applications”, Prentice Hall, 1995,
3. Chandra Mohan “An Introduction to Fuzzy Set Theory and Fuzzy Logic”, MV Learning, 2015
4. Kazuo Tanaka, “An Introduction to Fuzzy Logic for Practical Applications”, Springer, 1996

VED-558 NEURAL NETWORKS

Historical concepts of artificial neural networks, artificial neurons, neural networks and architectures, supervised and unsupervised learning methods, Radial Basis Function (RBF) neural networks, Recurrent Neural Networks(RNN),Hopfield neural networks, Adaptive resonance theory, Self organizing feature maps, Neural networks and soft computing paradigm, Engineering applications of Neural network, VLSI implementation of Neural network.

References:

1. Simon Haykin, “Neural Networks: A Comprehensive Foundations”, MacMillan Publishing Company, 1994
2. Satish Kumar, “Neural Networks: A Classroom Approach”, McGraw Hill Education, 2004
3. Mohamad Hassoun, “Fundamentals of Artificial Neural Networks”, MIT Press, 2003

VED-514 VLSI LAB

Design Simulation and implementation of digital and analog circuits using Xilinx tools and hardware

VED 524 SYSTEM DESIGN LAB

Designing and simulation of CMOS digital and analog circuits using CADENCE, SYNOPSIS and MENTOR GRAPHICS Tools