Brief Report of Conference

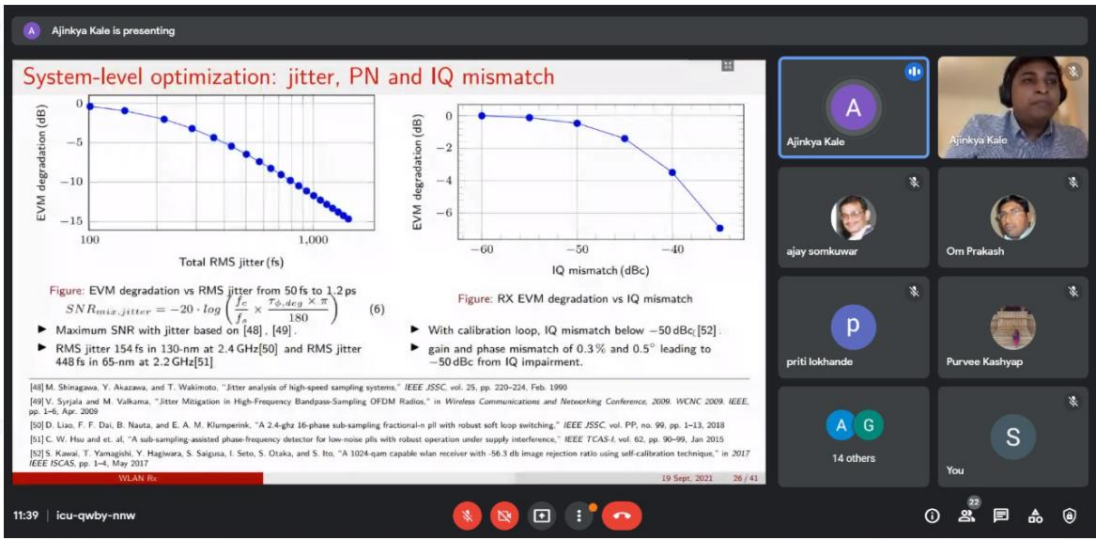
National Conference on Emerging Technologies in Intelligent Electronic System Design (ETIES) was conducted by department of Electronics and Communication Engineering, Maulana Azad National Institute of Technology, Bhopal. It was a two day conference from September 18 to 19 , 2021.

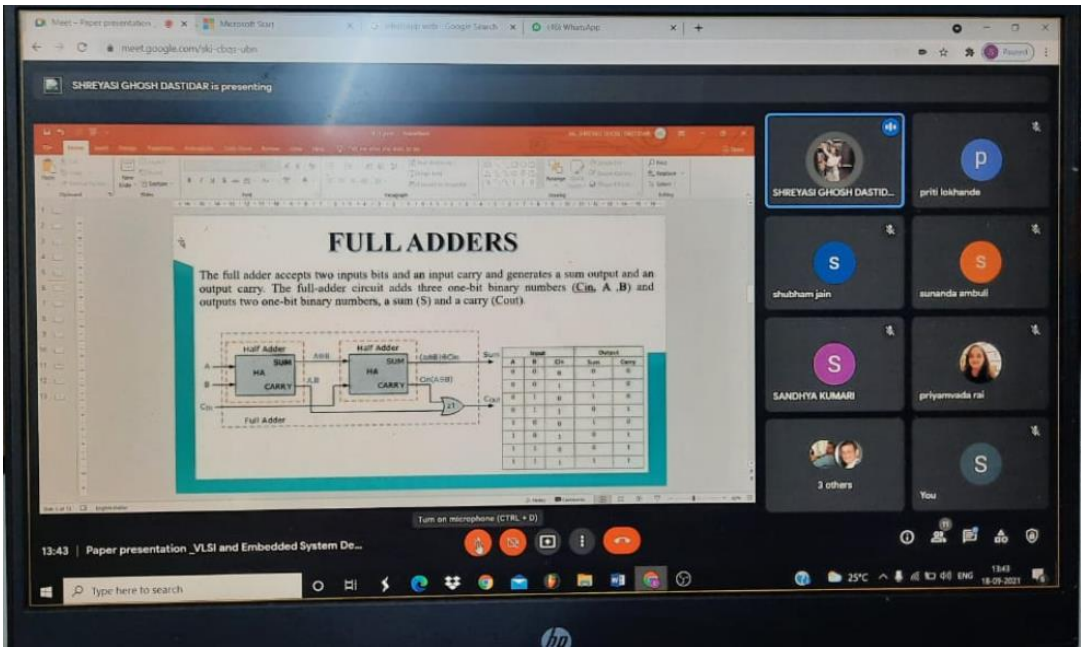
The conference was chaired by Dr. Ajay Somkuwar (Dept. of ECE, MANIT Bhopal). Keynote talk in the conference was delivered by Dr. Sanjeet Kumar Diwedi (Danfoss Power Electronics A/S Control Engineering Global R & D Design Centre Denmark). There were three parallel sessions in the conference. Session A for "VLSI and Embedded System Design" chaired by Dr. Sangeeta Nakhate (Dept. of ECE, MANIT Bhopal) & Dr. Sunanda Ambulkar (Dept. of ECE, NIT Puducherry), Session B for "Communication Engineering" chaired by Dr. O. P. Meena (Dept. of ECE, MANIT Bhopal) & Dr. Arjun Singh Yadav (Dept. of ECE, NIT Rourkela) and Session C for "Signal Processing" chaired by Dr. Manish Kashyap (Dept. of ECE, MANIT Bhopal) & Dr. Nisha Chaurasia (Dept. of IT, NIT Jalandhar).

The conference completed successfully with presentation followed by discussion of 45 research papers (15 from MANIT & 30 from outside MANIT) presented by selected participants from various universities / organizations in the country.






Ajinkya Kale is presenting
System-level optimization: jitter, PN and IQ mismatch
EVM degradation (dB)
Total RMS jitter (fs)
Figure: EVM degradation vs RMS jitter from 50 fs to 1.2 ps
$SNR_{mix,jitter} = -20 \cdot log\left(\frac{f_c}{f_x} \times \frac{\tau_{\phi,deg} \times \pi}{180}\right)$ (6)
Maximum SNR with jitter based on [48] , [49] .
RMS jitter 154 fs in 130-nm at 2.4 GHz[50] and RMS jitter 448 fs in 65-nm at 2.2 GHz[51]
IQ mismatch (dBc)
Figure: RX EVM degradation vs IQ mismatch
With calibration loop, IQ mismatch below −50 dBc; [52] .
gain and phase mismatch of 0.3 % and 0.5° leading to −50 dBc from IQ impairment.
[48] M. Shinagawa, Y. Akazawa, and T. Wakimoto, "Jitter analysis of high-speed sampling systems," IEEE JSSC, vol. 25, pp. 220–224, Feb. 1990
[49] V. Syrjala and M. Valkama, "Jitter Mitigation in High-Frequency Bandpass-Sampling OFDM Radios," in Wireless Communications and Networking Conference, 2009. WCNC 2009. IEEE, pp. 1–6, Apr. 2009
[50] D. Liao, F. F. Dai, B. Nauta, and E. A. M. Klumperink, "A 2.4-ghz 16-phase sub-sampling fractional-n pll with robust soft loop switching," IEEE JSSC, vol. PP, no. 99, pp. 1–13, 2018
[51] C. W. Hsu and et. al, "A sub-sampling-assisted phase-frequency detector for low-noise plls with robust operation under supply interference," IEEE TCAS-I, vol. 62, pp. 90–99, Jan 2015
[52] S. Kawai, T. Yamagishi, Y. Hagiwara, S. Saigusa, I. Seto, S. Otaka, and S. Ito, "A 1024-qam capable wlan receiver with -56.3 db image rejection ratio using self-calibration technique," in 2017 IEEE ISCAS, pp. 1–4, May 2017
WLAN Rx
19 Sept, 2021
26 / 41
Ajinkya Kale
ajay somkuwar
Om Prakash
priti lokhande
Purvee Kashyap
14 others
You
11:39 | icu-qwby-nnw


SHREYASI GHOSH DASTIDAR is presenting
FULL ADDERS
The full adder accepts two inputs bits and an input carry and generates a sum output and an output carry. The full-adder circuit adds three one-bit binary numbers (Cin, A ,B) and outputs two one-bit binary numbers, a sum (S) and a carry (Cout).
Half Adder
Full Adder
SHREYASI GHOSH DASTID...
priti lokhande
shubham jain
sunanda ambuli
SANDHYA KUMARI
priyamvada rai
3 others
You
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13:43 | Paper presentation _VLSI and Embedded System De...
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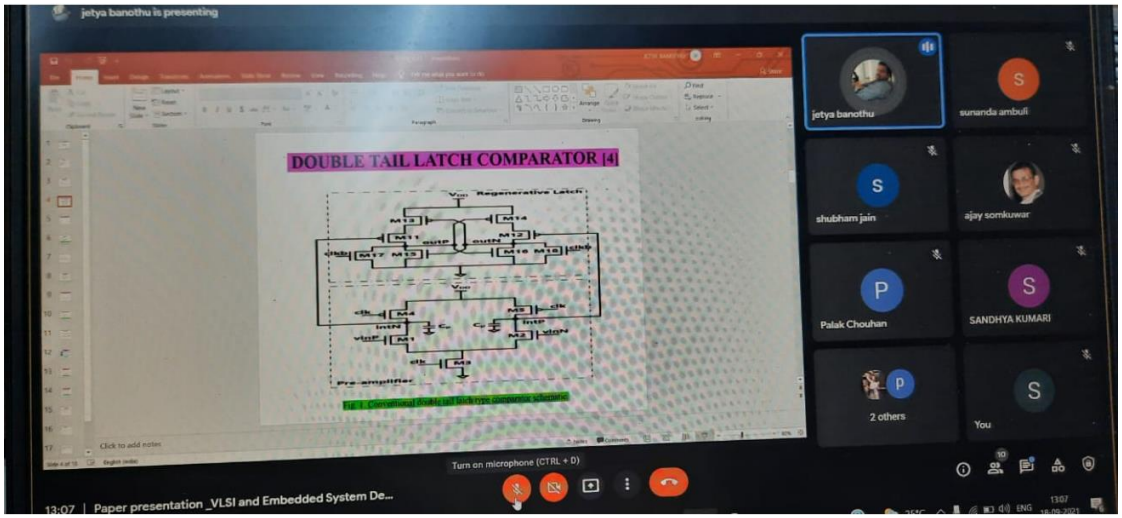
jetya banothu is presenting
DOUBLE TAIL LATCH COMPARATOR [4]
Regenerative Latch
Pre-amplifier
jetya banothu
sunanda ambuli
shubham jain
ajay somkuwar
Palak Chouhan
SANDHYA KUMARI
2 others
You
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13:07 | Paper presentation _VLSI and Embedded System De...